ABSTRACT

A digital signal processing system is disclosed that includes multiple processor subsystems, an external input/output port (XPORT), and an XPORT arbiter. The processor subsystems each include a processor core and a DMA controller, both of which may require access to the XPORT. The XPORT arbiter grants access by separately arbitrating between the processor cores and between the DMA controllers, and further arbitrating between processor control or DMA control of the XPORT. Upon receiving a request signal from a DMA controller, the XPORT arbiter asserts a hold signal to each of the processor cores. The processor cores respond to the hold signal by asserting a hold acknowledge signal. Note that if a processor core is currently using the XPORT, the processor core will delay assertion of the hold acknowledge signal until it is through with the XPORT. The arbiter, after receiving assertions of each of the hold acknowledge signals, then asserts a grant signal to the DMA controller requesting access. If both DMA controllers request access, only one at a time is provided with a grant signal assertion. Independently of the DMA controller arbitration, the arbiter may assert a grant signal to a processor core requesting access. However, the processor core's access will be stalled as long as the hold signal is asserted. Once the hold signal becomes de-asserted, the selected processor core may proceed with its access of the XPORT.